Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A microcomputer comprising:

a first memory where a normal-operation program is stored;

a second memory where a functional test program is stored;

a test mode detection circuit which monitors a signal supplied through an external terminal and detects if a test mode is designated;

a central processing unit (CPU) which accesses said first memory and runs said normal-operation program when said test mode is not designated, and accesses said second memory and runs said functional test program when said test mode is designated;

a memory management unit which monitors an access address and data with respect to said first and second memories and causes said CPU to execute a specific operation when there has been an unauthorized illegitimate access; and

a test circuit which [[gives]] sends a preset specific instruction to said CPU when, in said test mode, a security test signal has been output from said CPU and a specific memory area of said first and second memories has been accessed,

wherein the preset specific instruction is provided from a register within said test

circuit.

Claim 2 (Previously Presented): The microcomputer according to claim 1, wherein said specific instruction given to said CPU from said test circuit is an instruction which is to be detected by said memory management unit as an illegitimate access.

Claim 3 (Currently Amended): A microcomputer comprising:

a first memory where a normal-operation program is stored;

a second memory where a functional test program is stored;

a test mode detection circuit which monitors a signal supplied through an external terminal and detects if a test mode is designated;

a central processing unit (CPU) which accesses said first memory and runs said normal-operation program when said test mode is not designated, and accesses said second memory and runs said functional test program when said test mode is designated;

a memory management unit which monitors an access address and data with respect to said first and second memories and causes said CPU to execute a specific operation when there has been an unauthorized illegitimate access; and

an exception processing circuit, included in said CPU, for executing a predetermined exception process responsive to a signal indicative of an unauthorized illegitimate access of said first and second memories when said functional test program

is executing a security test and said memory management unit has instructed execution of said specific operation.

Claim 4 (Canceled)